Reckless Speeding

The investigation of the programming capabilities of the HAL hypercomputer

Reese Dandawate
Governor's School
NASA mentorship
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An Overview of the HAL hypercomputer

- A revolutionary new computer that makes computing dramatically faster
- Parallel Processing
- FPGAs- hardware
- VIVA- operating environment
- Many advantages over traditional CPUs
- Great potential for future

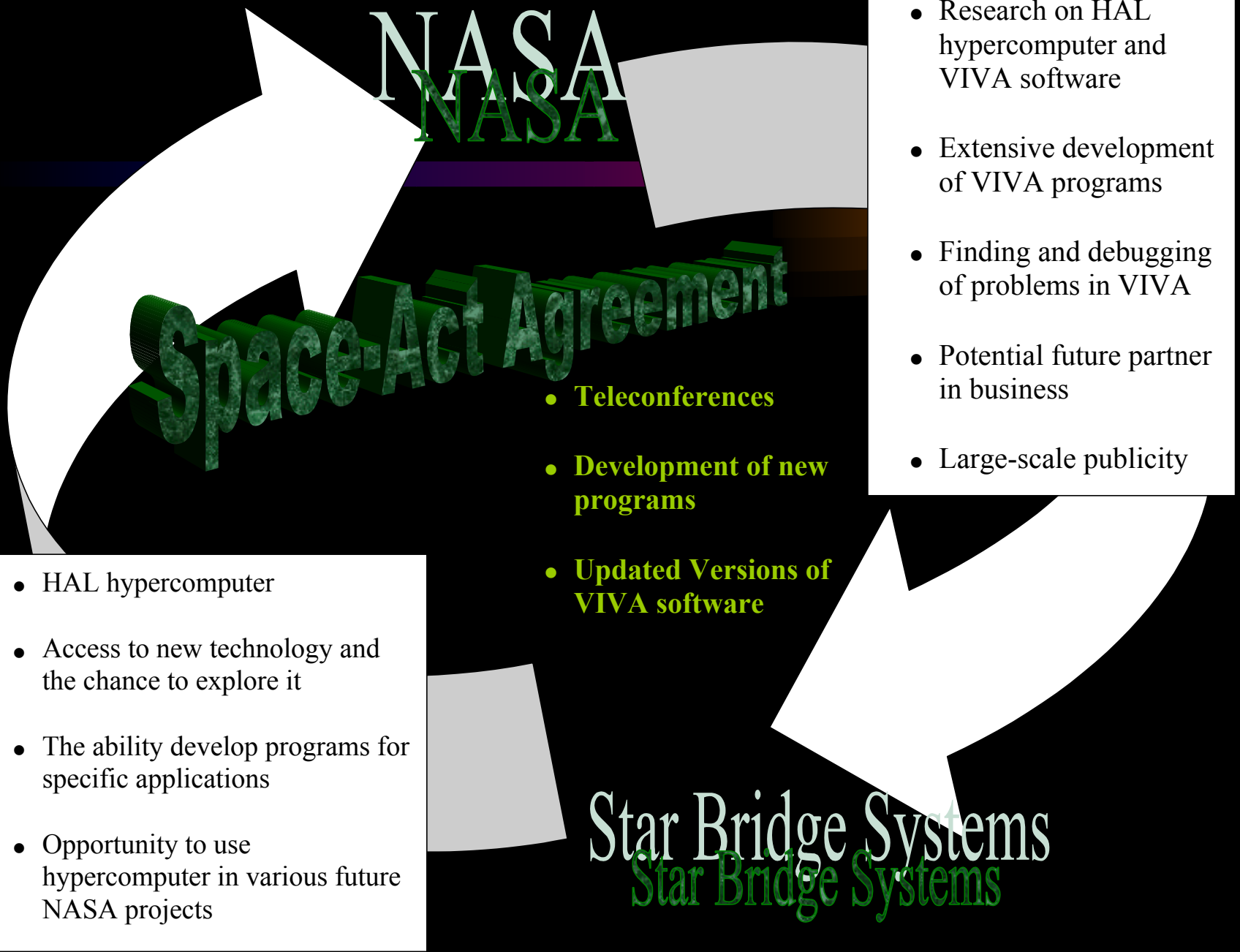
HAL hypercomputer

- **H**yper **A**lgorithmic **L**ogic hypercomputer
- Primary Advantage: SPEED
- Two types: HAL-15 and HAL-300GrW1
- Cost: HAL-15 - $1 million

  HAL-300GrW1 - $26 million
- Created by Star Bridge Systems

Star Bridge Systems

- Utah-based company
- Kent Gilson
- Dedicated to the development of “reconfigurable computing”
- NASA
  - Space-Act Agreement


NASA
NASA
Space-Act Agreement
Teleconferences
Development of new programs
Updated Versions of VIVA software
Research on HAL hypercomputer and VIVA software
Extensive development of VIVA programs
Finding and debugging of problems in VIVA
Potential future partner in business
Large-scale publicity
HAL hypercomputer
Access to new technology and the chance to explore it
The ability develop programs for specific applications
Opportunity to use hypercomputer in various future NASA projects
Star Bridge Systems
Star Bridge Systems

Parallel Processing

- Traditional computers- Serial Processing
- HAL hypercomputer- Parallel Processing

  Parallel Processing- the ability to execute numerous task simultaneously

- Possible because of FPGAs

FPGAs

- **F**ield **P**rogrammable **G**ate **A**rray chips
- HAL – 10 FPGAs per hypercomputer
- Pieces of silicon with millions of gates
- Able to be reprogrammed based on the task on hand- creates “specialized CPU”
- Able to be reprogrammed 1000 times per second
- Unused FPGAs may work on other tasks
- Takes full advantage of an algorithms inherent parallel nature

Year 2: Exploit Latest FPGAs

Rapid Growth in FPGA Capability

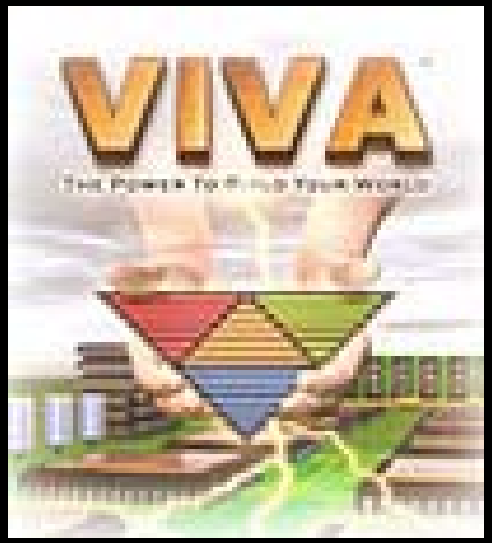
	FPGA (Feb '01)	FPGA (Aug '02)
Xilinx FPGA	XC4062	XC2V6000
Gates	62K	6 million (97x)
Multiplies in H/W	0	144 (18x18)
Clock Speed MHz	100	300 (3x)
Memory	20Kb	3.5 Mb (175x)
Memory Speed	466 Gb/s	5 Tb/s (11x)
Reconfigure Time	100ms	40ms (2.5x)
GFLOPS	0.4	47 (120x)
Total GFLOPs	**4** (10 FPGAs)	**470** (10 FPGAs)

Plans:

- Millions of Matrix Equations for Structures, Electromagnetics & Acoustics
- Rapid Static & Dynamic Structural Analyses
- Cray Vector Computations in Weather Code (VT PhD)
- Robert on Administrator's Fellowship at Star Bridge Systems
- Joint proposals with NSA & DARPA planned
- Simulate advanced computing concepts using VIVA
- Collaborate with SBS to expand VIVA libraries
- Influence VIVA development to meet NASA application needs
- Expand FPGA applications for NASA programs

VIVA software

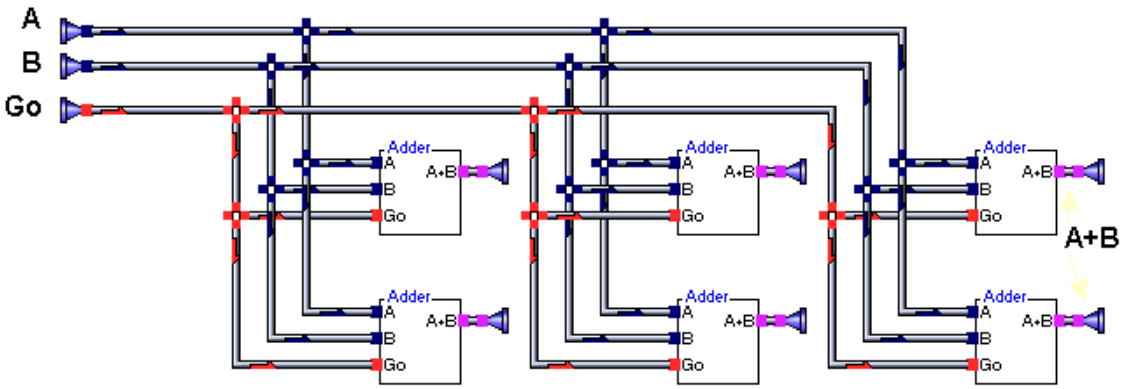
- What: Graphical Programming Language
- How: Transforms high-level graphical code to logical circuitry
- Why: Achieves near ASIC speed
- VIVA is learned through:
  - Training Conferences (March 2001)
  - Web site (www.progressforge.com)



Viva 2.0

Project Executable Sheet Edit View System Tools Help

MetaLib



New Project
MetaLib

Basic Data Sets
COM Data Sets
Primitive Objects
Input
Output
$Select
AND
DeRef
INVERT
OR
Ref
Release
Text
Composite Objects
Control
Convert
DataInfo
ExposeCollect
Gates
I/O
Math
Memory
Mux
Registers
Shifting
TestSheets

I2ADL Editor | Data Set Editor

Project | System | COM

Start | C:\Viva | Viva 2.0 | 2:58 PM

*Langley Algorithms Developed**

- **Matrix Algebra**: Vectors, Matrices, Dot Products
- **Factorial** => Probability: Combinations/Permutations AIRSC
- **Cordic** => Transcendentals: sin, log, exp, cosh…
- **Integration & Differentiation** (numeric)
- **Matrix Equation Solver**: [A]{x} = {b} via Gauss & Jacobi
- **Dynamic Analysis**: $[M]\{\ddot{u}\} + [C]\{\dot{u}\} + [K]\{u\} = \{P(t)\}$
- **Nonlinear Analysis**: Structural Analysis
- **Analog Computing**: Algorithm exploitation

* In *AIAA* & *Military & Aerospace Programmable Logic Device (MAPLD)* papers

Growth Capability in VIVA

VIVA 1 February 2001

- **NO** Floating Point
- **NO** Scientific Functions
- **NO** File Input/Output
- **NO** Vector-Matrix Support
- Access to **One** FPGA
- **Primitive** Documentation
- Weekly Changes
- Frequent “bugs”

VIVA 2 July 2002

- **Extensive** Data Types
- Trig, Logs, Transcendentals
- File Input/Output
- Vector-Matrix Support
- Access to **Multiple** FPGAs
- **Extensive** Documentation
- Stable Development
- Few “bugs”

CPU vs. HAL

Traditional CPU

Sequential: 1 operation/cycle

Fixed gates & data types

Wasteful: 99% gates idle/cycle

yet all draw power

Software: Text

```
do i = 1, billion
    c= a+b
    end do
```

26 MFLOPS/250 MHz SGI

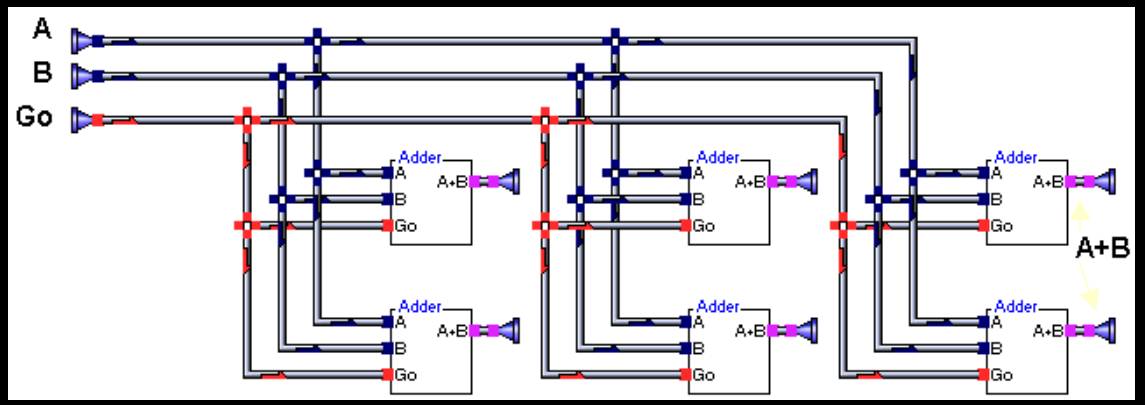
Reconfigurable FPGA

Parallel: Inherent

Dynamic gates & data types

Efficient: Optimizes gates to task

Gateware: VIVA Icons & Transports



392+ MFLOPS/64 MHz FPGA

3.92+ GFLOPS/10 FPGA board

HAL in NASA

- Spacecraft and Satellite control centers
- Solutions for structural, electromagnetic and fluid analysis
- Radiation analysis for astronaut safety
- Atmospheric science analysis
- Digital signal processing
- Pattern recognition
- Acoustic analysis

HAL in the community

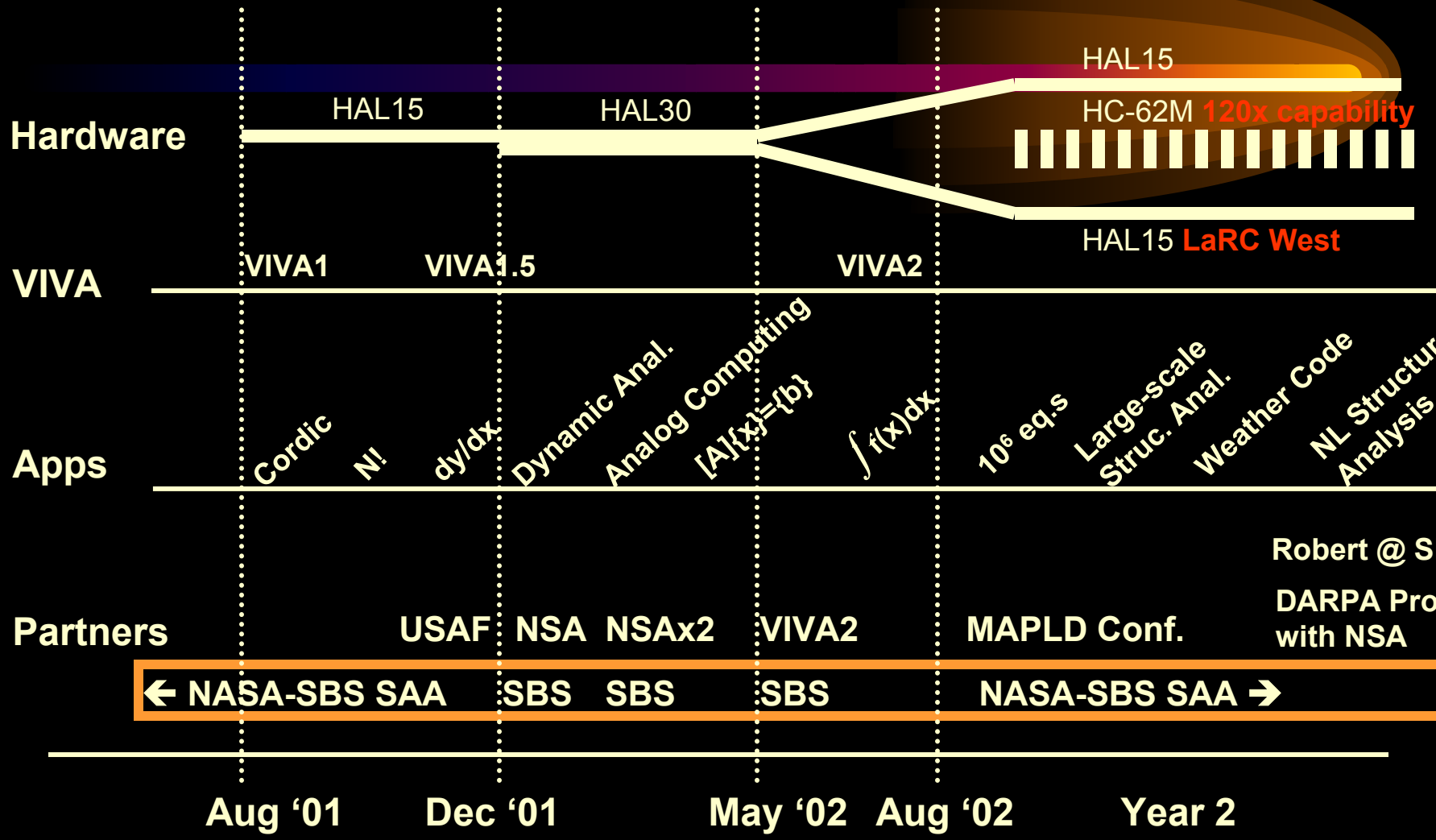
Currently

- **The execution of the largest virtual supernova experiment**
- **The creation of a large-scale hypercomputer**

Future

- **Gene Mapping**
- **Mainframe and personal computers**
- **Virtual Simulation**
- **Film special effects**

Progress – Roadmap

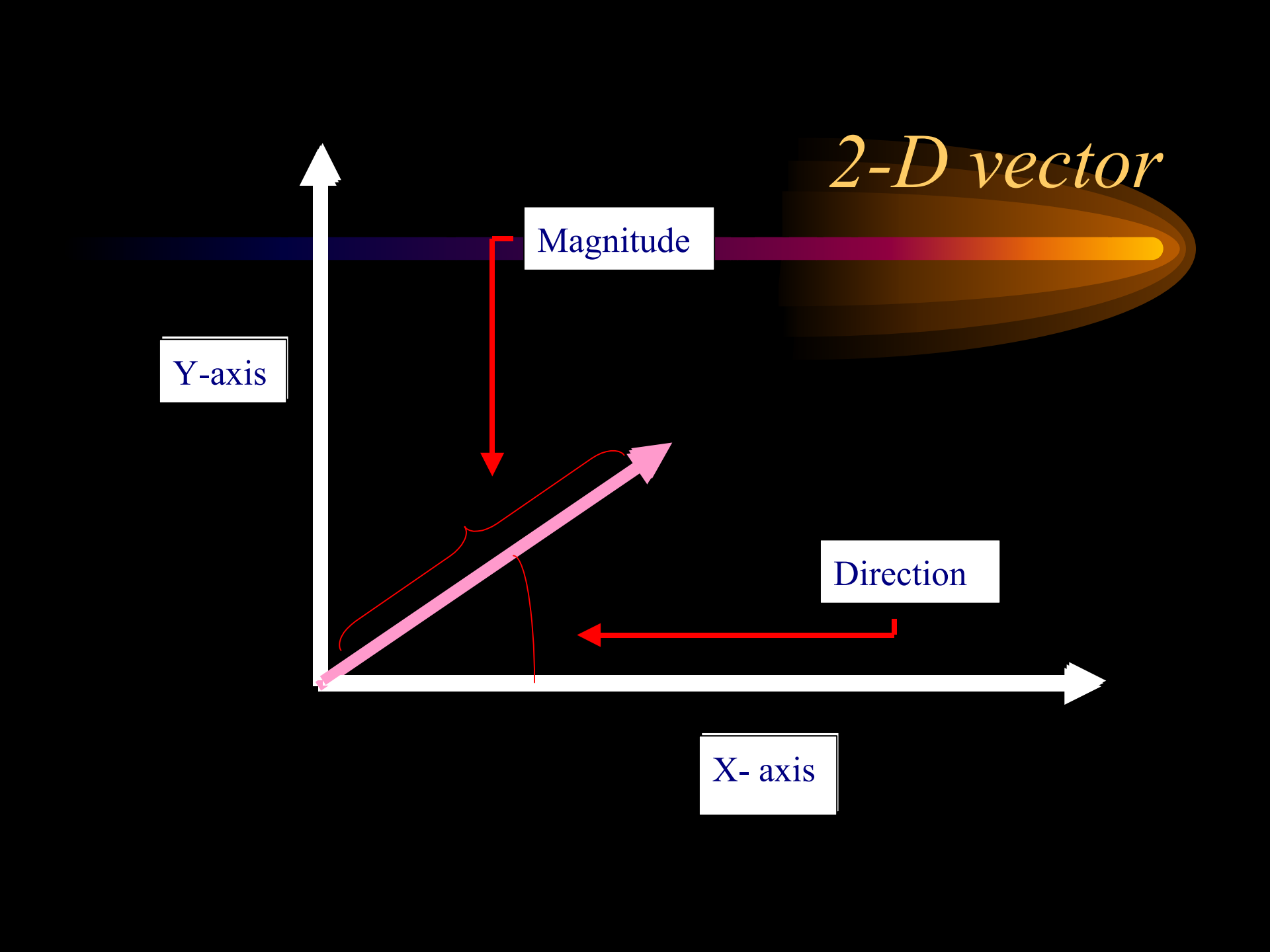


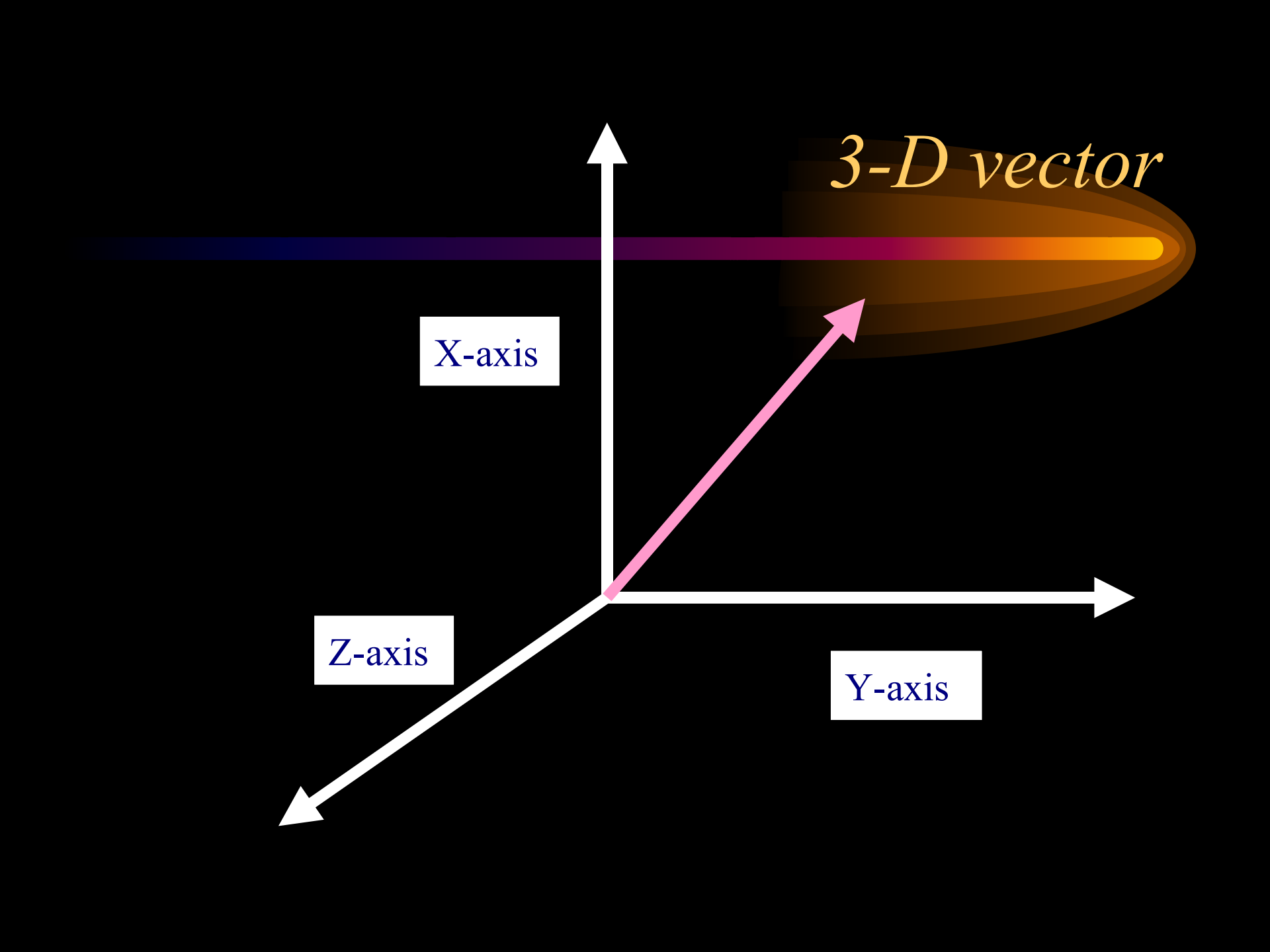
My project

- Get familiar with VIVA and HAL
- Develop vector product
- Find problems within the system

What is a vector?

- A ray with magnitude and direction


2-D vector
Magnitude
Y-axis
Direction
X- axis


3-D vector
X-axis
Z-axis
Y-axis

Vector Cross Product

- Cramer's Rule
- Why created…

Debugging the HAL

- Finding bugs with the program
- Square Root Function

Special Thanks to...

- Dr. Storaasli
- William Fithian
- Siddharta Krishnamurthy

The End

Any questions?